FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.

1875.2790002/RES/GSB

APPLICATION NO.

TO Be Assigned

APPLICANT

Jan MULDER

FILING DATE
Herewith (October 21, 2003)
TO Be Assigned

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EXAMINER INITIAL		DOC NUM	UMENT BER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE	
1310	AA1	6,4	89,913	12/2002	Hansen et al.	341	156		
	AB1	5,9	73,632	10/1999	Tai	341	156		
	AC1	6,2	59,745 B1	07/2001	Chan	375	285		
V	AD1	5,1	91,336	03/1993	Stephenson	341	111		
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	AL1							Yes No	
	AM1							Yes No	
	AN1				_			Yes No	
	A01							Yes No	
	AP1							Yes No	
		-	OTHER (Incl	uding Author.	Title, Date, Pertinent Pa	ges. etc.)			
BIO	AR	1	Abo, A.M. Digital Co	and Gray, P.R	., "A 1.5-V, 10-bit, 14.3- E Journal of Solid-State C	MS/s CMOS	Pipeline A	nalog-to- 34, No. 5,	
	AS	<u>1</u>	Brandt, B.P. and Lutsky, J., "A 75-mW, 10-b, 20-MSPS CMOS Subranging ADC with 9.5 Effective Bits at Nyquist," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 34, No. 12, December 1999, pp. 1788-1795.						
V	Bult, Klaas and Buchwald, Aaron, "An Embedded 240-mW 10-b 50-MS/s CMOS ADC in 1-mm²," IEEE Journal of Solid-State Circuits, IEEE, Vol. 32, No. 12, December 1997, pp. 1887-1895.								
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			OTHER (Incl	uding Author,	Title, Date, Pertinent Pag	es, etc.)	·		
BK	OTHER (Including Author, Title, Date, Pertinent Pages, etc.) Cho, T.B. and Gray, P.R., "A 10 b, 20 Msample/s, 35 mW Pipeline A/D Converter," IEEE Journal of Solid-State Circuits, IEEE, Vol. 30, No. 3, March 1995, pp. 166- 172.								
	AS	<u>2</u>	Choe, M-J. et al., "A 13-b 40-Msamples/s CMOS Pipelined Folding ADC with Background Offset Trimming," IEEE Journal of Solid-State Circuits, IEEE, Vol. 35, No. 12, December 2000, pp. 1781-1790.						
J	AT 1	<u>2</u>	Choi, M. and Abidi, A., "A 6-b 1.3-Gsample/s A/D Converter in 0.35-\mu CMOS," IEEE Journal of Solid-State Circuits, IEEE, Vol. 36, No. 12, December 2001, pp. 1847-1858.						
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	1	<u> </u>	OTHER (Incl	uding Author	Title Date Portinent Dec	ree etc.)		1 10		
BI	OTHER (Including Author, Title, Date, Pertinent Pages, etc.) Flynn, M. and Sheahan, B., "A 400-Msample/s, 6-b CMOS Folding and Interpolating ADC," IEEE Journal of Solid-State Circuits, IEEE, Vol. 33, No. 12, December 1998, pp. 1932-1938.									
	AS	<u>3</u>	Geelen, G. State Circ	Geelen, G., "A 6b 1.1GSample/s CMOS A/D Converter," IEEE International Solid- State Circuits Conference, IEEE, 2001, pp. 128-129 and 438.						
	AT /	<u>3</u>	Hoogzaad, G. and Roovers, R., "A 65-mW, 10-bit, 40-Msample/s BiCMOS Nyquist ADC in 0.8 mm²," IEEE Journal of Solid-State Circuits, IEEE, Vol. 34, No. 12, December 1999, pp. 1796-1802.							
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BIN	AR	<u>4</u>	Hosotani, Consumptio	S. et al., "A	un 8-bit 20-MS/s CMOS A/D C cnal of Solid-State Circuit	onverter w		
	Ingino, J.M. and Wooley, B.A., "A Continuously Calibrated 12-b, 10-MS/s, 3.3-V A/D Converter," IEEE Journal of Solid-State Circuits, IEEE, Vol. 33, No. 12, December 1998, pp. 1920-1931.							
	AT 4 Ito, M. et al., "A 10 bit 20 MS/s 3 V Supply CMOS A/D Converter," IEEE Journal of Solid-State Circuits, IEEE, Vol. 29, No. 12, December 1994, pp. 1531-1536.							
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Blir	OTHER (Including Author, Title, Date, Pertinent Pages, etc.) Kattman, K. and Barrow, J., "A Technique for Reducing Differential Non-Linearity Errors in Flash A/D Converters," IEEE International Solid-State Conference, IEEE, 1991, pp. 170-171.								
	AS	Kusumoto, K. et al., "A 10-b 20-MHz 30-mW Pipelined Interpolating CMOS ADC," IBEE Journal of Solid-State Circuits, IEEE, Vol. 28, No. 12, December 1993, pp. 1200-1206.							
V	AT	<u>5</u>	Lewis, S. et al., "A 10-b 20-Msample/s Analog-to-Digital Converter," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 27, No. 3, March 1992, pp. 351-358.						
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Blr	OTHER (Including Author, Title, Date, Pertinent Pages, etc.) Mehr, I. and Singer, L., "A 55-mW, 10-bit, 40-Msample/s Nyquist-Rate CMOS ADC," IEEE Journal of Solid-State Circuits, IEEE, Vol. 35, No. 3, March 2000, pp. 318-325.							
	Nagaraj, K. et al., "Efficient 6-Bit A/D Converter Using a 1-Bit Folding Front End," IEEE Journal of Solid-State Circuits, IEEE, Vol. 34, No. 8, August 1999, pp. 1056-1062.						ing Front ust 1999,	
	Nagaraj, K. et al., "A Dual-Mode 700-Msamples/s 6-bit 200-Msamples/s 7-bit A/D Converter in a 0.25-\(\mu\)m Digital CMOS," IEEE Journal of Solid-State Circuits, IEEE, Vol. 35, No. 12, December 2000, pp. 1760-1768.							
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BM	AR	2	Converter,	and Venes, A. " IEEE Journa 1302-1308.	, "A 70-MS/s 110-mW 8-b CMC l of Solid-State Circuits,	S Folding IEEE, Vol.	and Inter	polating A/D 12, December
	Pan, H. et al., "A 3.3-V 12-b 50-MS/s A/D Converter in 0.6-μm CMOS with over 80-dB SFDR," IEEE Journal of Solid-State Circuits, IEEE, Vol. 35, No. 12, December 2000, pp. 1769-1780.							
Song, W-C. et al., "A 10-b 20-Msample/s Low-Power CMOS ADC," IEEE Journal of Solid-State Circuits, IEEE, Vol. 30, No. 5, May 1995, pp. 514-521.								rnal of
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BIV	OTHER (Including Author, Title, Date, Pertinent Pages, etc.) Sumanen, L. et al., "A 10-bit 200-MS/s CMOS Parallel Pipeline A/D Converter," IEEE Journal of Solid-State Circuits, IEEE, Vol. 36, No. 7, July 2001, pp. 1048- 1055.								
d d	Taft, R.C. and Tursi, M.R., "A 100-MS/s 8-b CMOS Subranging ADC with Sustained Parametric Performance from 3.8 V Down to 2.2 V," IEEE Journal of Solid-State Circuits, IEEE, Vol. 36, No. 3, March 2001, pp. 331-338.								
	van der Ploeg, H. and Remmers, R., "A 3.3-V, 10-b 25-Msample/s Two-Step ADC in 0.35-μm CMOS," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 34, No. 12, December 1999, pp. 1803-1811.								
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BW	OTHER (Including Author, Title, Date, Pertinent Pages, etc.) van der Ploeg, H. et al., "A 2.5-V 12-b 54-Msample/s 0.25-μm CMOS ADC in 1-mm² With Mixed-Signal Chopping and Calibration," IEEE Journal of Solid-State Circuits, IEEE, Vol. 36, No. 12, December 2001, pp. 1859-1867.							
	Vorenkamp, P. and Roovers, R., "A 12-b, 60-Msample/s Cascaded Folding and Interpolating ADC," IEEE Journal of Solid-State Circuits, IEEE, Vol. 32, No. 12, December 1997, pp. 1876-1886.							and 32, No. 12,
V	Wang, Y-T. and Razavi, B., "An 8-bit 150-MHz CMOS A/D Converter," IEEE Journal of Solid-State Circuits, IEEE, Vol. 35, No. 3, March 2000, pp. 308-317.							
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	AP10							Yes No	
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BW	Yotsuyanagi, M. et al., "A 2 V, 10 b, 20 Msample/s, Mixed-Mode Subranging CMOS A/D Converter," IEEE Journal of Solid-State Circuits, IEEE, Vol. 30, No. 12, December 1995, pp. 1533-1537.								
	AS	<u>10</u>	Yu, P.C. and Lee, H-S., "A 2.5-V, 12-b, 5-Msample/s Pipelined CMOS ADC," IEEE Journal of Solid-State Circuits, IEEE, Vol. 31, No. 12, December 1996, pp. 1854-1861.						
	AT	10	10b Pipeli	Miyazaki et al., ISSCC 2002/Session 10/High-Speed ADCs/10.5, "A 16mW 30 MSample/s 10b Pipelined A/D Converter using a Pseudo-Differential Architecture", February 5, 2002, 3 pgs.					
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OTHER (Including Author, Title, Date, Pertinent Pages, etc.) AR 11 Sushihara et al., ISSCC 2002/Session 10/High-Speed ADCs/10.3, "A 7b 450 MSample/s 50mW CMOS ADC in 0.3 mm2", February 5, 2002, 3 pgs.									
m	AS	11	Dingwall e	Dingwall et al., IEEE Journal of Solid-State Circuits, Vol. SC-20, No. 6, "An 8- MHz CMOS Subranging 8-Bit A/D Converter", December 1985, pgs. 1138-1143.					
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